Patent Claims

1. A synchronous integrated memory,

- having a control unit (CTR) for producing a first internal clock (CLKI1), which leads the external clock (CLKE) by a specific phase shift (ΔTOUT),
- having an output circuit (OUT),
- which can be activated via an activation input (AKT),
- which, in the activated state, starts an output process for the data (D) to be read out, in synchronism with the first internal clock (CLKI1),
- and which outputs the data (D) with the specific phase shift (ΔTOUT) with respect to the first internal clock (CLKI1), that is to say in synchronism with the external clock (CLKE), at the data connection (P),
- having a clock generator (G) for a second internal clock (CLKI2), which is synchronized to the external clock (CLKE),
- having a counting unit (CT),
- which starts a counting process for recording the number of successively following first levels of the first internal clock (CLKI1) as soon as the second internal clock (CLKI2) for the first time assumes a first level while an output control signal (PAR) is at a first level,
- and which activates the output circuit (OUT) via its activation input (AKT) as soon as the number of successively

following first levels of the first internal clock (CLKI1) has reached a predetermined value.

2. The integrated synchronous memory as claimed in claim 1, whose counting unit (CT) is supplied with a variable control signal (L) via which different predetermined values can be set for the number of successively following first levels of the first internal clock (CLKI1).

3. The integrated synchronous memory as claimed in claim 2,

whose counting unit (CT) has a shift register with a series circuit of register elements (RE),

in which one input of the first register element (RE) of the series circuit is supplied with the output control signal (PAR),

whose first register element (RE) is clocked by the second internal clock (CLKI2) and whose other register elements (RE) are clocked as a function of the first internal clock (CLKI1),

having a multiplexer (MUX), via which the outputs of at least some of the register elements (RE) are connected to the activation input of the output circuit (OUT) and whose switching state can be set via the control signal (L).

4. The integrated synchronous memory as claimed in one of the preceding claims, whose clock generator (G) produces the second internal clock (CLKI2) from the first internal clock, by means of a delay element.

5. The integrated synchronous memory as claimed in claim 4, -- whose control unit (CTR) has an input which is connected to the external clock (CLKE) and an output to which the input is connected via a variable delay unit (DEL) and at which it produces the first internal clock (CLKI1),
- and whose control unit (CTR) has a phase comparator (φ) with a first input which is connected to the input of the control unit, with a second input to which the output of the control unit is connected via the delay element of the clock generator (G), and with an output which is connected to a control input of the delay unit (DEL).